REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-28 are pending in the application.

Claims 1-28 are rejected.

35 U.S.C. § 103

In the above-referenced office action, the Examiner asserts the following:

"5. Claims 1-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherubini et al. (US 6,741,551) in view of McCallister et al. (US 6,005,897)." (office action, Part of Paper No./Mail Date 20081228, p. 4)

The Applicant respectfully traverses.

The Applicant has amended certain of the claims.

On page 3 of the office action, the Examiner states:

"**Examiner's response:** In figure 3, McCallister et al. clearly illustrates that encoder 56 produces six encoded bits or symbols (s) in response to the three information bits processed by the PARSE 30. The output of the encoder 56 is input to Transparent Convolutional Encoder 62. The encoder 62 produces corresponding symbol pairs for the data streams in which either both symbols are inverted or neither symbol is inverted. This clearly shows "rearranging" the order of information bits coming out of the PARSE 30 from 3 information bits to six information bit which is performed by encoder 56 and also encoder 56 (see figure 3 below and col 6, lines 39-67, col 7, lines 1-67." (emphasis added)

Firstly, the Applicant respectfully points out that "symbol pairs for the data streams in which either both symbols are inverted or neither symbol is inverted" is not rearranging of an order of a plurality of encoded bits.

Inversion or inverting, in digital signal processing, means to change a value of a bit from its true value to its complementary value (e.g., true bit value "1" changed to bit value "0", or true bit value "0" changed to bit value "1"). This is consistent with McCallister's use of the term (e.g., "causes the encoded bits to become inverted from

their true values" in col. 14, lines 2-3; "encoded bits are detected in their inverted state" in col. 14, line 6; "inverted from their true states" in col. 18, lines 7-9; etc.).

As an example, the inverted value of a 3-bit symbol "111" would be "000". As such, the inverted symbol "000" is not a order-rearranged version of the true symbol value "111", because the bit values "111" are no longer even present in the inverted symbol "000". Therefore, inversion or inverting of a bit or symbol is not rearranging of any order in accordance with the subject matter as claimed by the Applicant.

Also, in contrast to the Examiner's analysis in "**Examiner's response**" cited above, McCallister teaches and discloses that it is the encoding as performed by convolutional encoder 62 that produces "six encoded bits or symbols(s)" based on "three information bits processed" because it is a rate 1/2 encoder.

McCallister teaches and discloses:

"An output of differential encoder 56 couples to an input of a convolutional encoder 62. In the preferred embodiment, encoder 62 implements a transparent, recursive, K=7, rate 1/2 convolutional ("Viterbi") encoder. Encoder 62 may implement either a systematic or non-systematic code. Since encoder 62 implements a rate 1/2 code, two symbols (s) are produced for each information bit received from differential encoder 56. Over the above-discussed two unit interval period, six encoded bits or symbols(s) are produced in response to the three information bits processed. FIG. 3 denotes the two symbols produced for each information bit processed by using the subscripts "0" and "1"." (McCallister, col. 7, lines 39-51, emphasis added)

McCallister's rate 1/2 encoder will produce 2x output bits based on x input bits (e.g., the number of output bits is equal to twice the number of input bits within a rate 1/2 encoder).

Moreover, the Applicant also respectfully points out that the bits input to the encoder 62 (depicted by letter "d") are not the same as the bits output from the encoder 62 (depicted by letter "s") (see also McCallister's specific distinction between "data bits" input thereto and "encoded bits or symbols" output there from).

However, on page 6 of the office action, the Examiner asserts:

"However, McCallister et al., in the same field of endeavor teaches encoding a plurality of information bits, thereby generating a plurality of encoding bits (52, 56, 62 in

figure 3); rearranging an order of the plurality of encoded bits, thereby generating a sequence of discrete-valued modulation symbols (see in figure 3 that the PARSE 30 which produces 3 information bits and the encoder 56 and 62 produces 6 information bit in response to the 3 information bit. The examiner is making his broadest reasonable interpretation that the producing 6 information bits in response to 3 information bits to be rearranging an order of the plurality of encoded bits) (62, 64, 68 in figure 3 and col 7, lines 59-67, col 8, lines 1-65)." (emphasis added)

Rather, as cited above from McCallister, it is the encoding therein (as performed by the encoder 62) that produces "six encoded bits or symbols(s)" (i.e., not 6 information bits as Examiner asserts) from the "three information bits processed".

This is because, as cited above, "encoder 62 implements a rate 1/2 code, two symbols (s) are produced for each information bit received from differential encoder 56. Over the above-discussed two unit interval period, six encoded bits or symbols(s) are produced in response to the three information bits processed".

The Applicant respectfully asserts that to construe the straight-forward teaching and disclosure of McCallister's encoding (performed by "encoder 62") using a "rate 1/2 code" to be rearranging an order of the plurality of encoded bits is improper.

McCallister's encoder 62 simply performs encoding (i.e., "six encoded bits or symbols(s) are produced in response to the three information bits processed"), and not any rearranging an order of the plurality of encoded bits.

Again, McCallister's rate 1/2 encoder will produce 2x output bits based on x input bits (e.g., the number of output bits is equal to twice the number of input bits within a rate 1/2 encoder). For example, if x="three information bits" as in McCallister, then 2x="six encoded bits or symbols(s) are produced in response to the three information bits processed."

This is straight-forward encoding in McCallister, and it is not rearranging any order of either the "three information bits" or the "six encoded bits or symbols(s)".

Moreover, looking at McCallister's FIG. 3, the order of encoded bits output from the encoder 62 is exactly the same as the order of the data bits input to the encoder 62 (e.g., look at the superscripts thereof).

For example, in McCallister's FIG. 3, because "two symbols (s) are produced for each information bit received from differential encoder 56", when the input corresponding to bit "d_1^0" is provided from the differential encoder 56 to the encoder 62, the encoder 62 generates output bits "s_1^0" and "s_0^0"; note the very same superscript to all bits (no rearrangement of order).

Analogously, when the input corresponding to bit "d_1^3" is provided from the differential encoder 56 to the encoder 62, the encoder 62 generates output bits "s_1^3" and "s_0^3"; note the very same superscript to all bits (no rearrangement of order).

Analogously, when the input corresponding to bit "d_1^4" is provided from the differential encoder 56 to the encoder 62, the encoder 62 generates output bits "s_1^4" and "s_0^4"; note the very same superscript to all bits (no rearrangement of order).

As a function of order, as shown by the superscripts of these bits in McCallister's FIG. 3, it can be seen that the superscript indicating order of bits being input to the encoder 62 is "4 3 0" and the superscript indicating order of bits being output from the encoder 62 is **exactly the same**, namely, "4 3 0".

In other words, the encoding of the "data bits" as performed by the encoder 62 maintains the very same order, in terms of superscript, within the "encoded bits or symbols(s)" output from the encoder 62 (i.e., each sequence has the very same order, namely, "4 3 0").

In addition, the operations of the encoder 62 is not rearranging of an order of encoded bits because the "encoded bits or symbols(s)" output from the encoder 62 are different bits (i.e., not the same) than the "data bits" provided as input to the encoder 62. [e.g., as described above, the bits input to the encoder 62 (depicted by letter "d") are not the same as the bits output from the encoder 62 (depicted by letter "s") (see also McCallister's specific distinction between "data bits" input thereto and "encoded bits or symbols" output there from)].

For example, "The zero-th data bit d.sub.1.sup.0 is converted by convolutional encoder 62 into encoded bits or symbols s.sub.1.sup.0 and s.sub.0.sup.0." (McCallister, col. 8, lines 2-3, emphasis added) Note that the superscript of the "encoded bits or symbols" is exactly the same as the superscript of the "data bit" ("sup.0") (i.e., there is no rearrangement of order there between).

The Applicant respectfully asserts that McCallister teaches and discloses that "data bits" are "converted by convolutional encoder 62 into encoded bits or symbols".

Conversion of bits in accordance with McAcllister's encoding is not the same as rearranging an order of the plurality of encoded bits (i.e., bits that have already been encoded: "plurality of encoded bits") in accordance with the subject matter as claimed by the Applicant.

When the Examiner asserts that "This clearly shows "rearranging" the order of information bits coming out of the PARSE 30 from 3 information bits to six information bit which is performed by encoder 56 and also encoder 56" or "The examiner is making his broadest reasonable interpretation that the producing 6 information bits in response to 3 information bits to be rearranging an order of the plurality of encoded bits) (62, 64, 68 in figure 3 and col 7, lines 59-67, col 8, lines 1-65)", the Examiner is improperly construing the straightforward teaching and disclosure of McCallister's encoding using a rate 1/2 code as rearranging an order of the plurality of encoded bits (again, as cited above, McCallister teaches and discloses that "Since encoder 62 implements a rate 1/2 code, two symbols (s) are produced for each information bit received from differential encoder 56. Over the above-discussed two unit interval period, six encoded bits or symbols(s) are produced in response to the three information bits processed").

Again, this encoding is a conversion process (not a rearrangement process), in that, the "encoded bits or symbols(s)" output from the encoder 62 are different bits (i.e., not the same) than the "data bits" provided as input to the encoder 62.

However, in McCallister's FIG. 3, the encoding of the "data bits" (having order "4 3 0") as performed by the encoder 62 maintains the very same order, in terms of superscript, within the "encoded bits or symbols(s)" output from the encoder 62 (i.e., each sequence has the very same order, namely, "4 3 0").

At best, McCallister's teaching and disclosure of "six encoded bits or symbols(s) are produced in response to the three information bits processed" could only be construed as encoding a plurality of information bits (e.g., "three information bits") thereby generating a plurality of encoded bits "six encoded bits or symbols(s) are produced".

Again, this encoding in McCallister is a conversion process in which the "encoded bits or symbols(s)" output from the encoder 62 are different bits (i.e., not the

same) than the "data bits" provided as input to the encoder 62, and as such, there is no rearranging of any order thereof (i.e., each sequence has the very same order, namely, "4 3 0", and there is no rearrangement of any order thereof).

When the Examiner states that "The examiner is making his broadest reasonable interpretation that the producing 6 information bits in response to 3 information bits to be rearranging an order of the plurality of encoded bits)", the Applicant respectfully points out that McCallister teaches and discloses that "six encoded bits or symbols(s) are produced in response to the three information bits processed" (in accordance with the encoding of encoder 62). The only coded bits in this reference of McCallister are the "six encoded bits or symbols(s)". The "three information bits" input are not encoded bits. Performing encoding of the "three information bits" to convert them to different bits, namely, the "six encoded bits or symbols(s)", is not rearrangement of any order of the "six encoded bits or symbols(s)".

Also, it is clear that McCallister performs puncturing of the "six encoded bits or symbols(s)" output from the encoder 62 in McCallister's FIG. 3.

The remaining non-punctured bits are then "s_1^4", "s_1^0" and "s_1^3", "s_0^0", and these bits are exactly the same bits that are provided to the P-APSK mapping circuit 68. There is therefore no rearranging an order of these non-punctured bits in McCallister's FIG. 3.

Moreover, in FIG. 3 of McCallister, the remaining punctured bits going into "puncture controller 64" are shown as $s_1^4\ s_1^3\ s_1^0$ (i.e., showing the 2nd bit, s_1^3, is to be punctured), and the output from the "puncture controller 64" is shown as $s_1^4\ s_1^0$.

The bit, s_1^0, precedes the bit, s_1^4, going into the "puncture controller 64", and the bit, s_1^0, precedes the bit, s_1^4, coming out of the "puncture controller 64". There is not a rearranging of the order of these two bits, $s_1^4\ s_1^0$, within the "puncture controller 64" or within the output from the "puncture controller 64".

If an order of these bits were rearranged, then the bit, s_1^0, would no longer precede the bit, s_1^4, coming out of the "puncture controller 64" (e.g., it would follow).

Also in FIG. 3 of McCallister, other bits going into "puncture controller 64" are shown as $s_0^4\ s_0^3\ s_0^0$ (i.e., showing the 1st bit, s_0^4, is to be punctured), and the output from the "puncture controller 64" is shown as $s_0^3\ s_0^0$.

The bit, s_0^0, precedes the bit, s_0^3, going into the "puncture controller 64", and the bit, s_0^0, precedes the bit, s_0^3, coming out of the "puncture controller 64". There is not a rearranging of the order of these two bits, s_0^3 s_0^0, within the "puncture controller 64" or within the output from the "puncture controller 64".

If an order of these bits were rearranged, then the bit, s_0^0, would no longer precede the bit, s_0^3, coming out of the "puncture controller 64" (e.g., it would follow).

The Applicant respectfully points out that McCallister performs timing management (e.g., "by delaying certain encoded bits as necessary"), but not order rearrangement in accordance with the subject matter as claimed by the Applicant (e.g., see comments above where order is same – "bit, s_0^0, precedes the bit, s_0^3, going into the "puncture controller 64", and the bit, s_0^0, precedes the bit, s_0^3, coming out of the "puncture controller 64"", etc.).

In an earlier action, the Examiner asserted "The Examiner is not limited to Applicant's definition, which is not specifically set forth in the claims".

Therefore, the Applicant has amended independent claims 1 and 13 to specifically set forth Applicant's definition of rearrangement related subject matter.

As can be seen in McAllister, there is no rearrangement of the order of any bits in accordance with the subject matter as claimed by the Applicant.

Again, on page 3 of the office action, the Examiner asserts that "In figure 3, McCallister et al. clearly illustrates that encoder 56 produces six encoded bits or symbols (s) in response to the three information bits processed by the PARSE 30. The output of the encoder 56 is input to Transparent Convolutional Encoder 62. The encoder 62 produces corresponding symbol pairs for the data streams in which either both symbols are inverted or neither symbol is inverted. This clearly shows "rearranging" the order of information bits coming out of the PARSE 30 from 3 information bits to six information bit which is performed by encoder 56 and also encoder 56".

As such, the Examiner equivalences McCallister's operations up to the output of the encoder 56 as ""rearranging" the order of information bits coming out of the PARSE 30 from 3 information bits to six information bit which is performed by encoder 56 and also encoder 56"" (an assertion that the Applicant traverses and respectfully asserts is improper).

However, the puncturing of McCallister is based on the output of the encoder 56 (i.e., on the "six encoded bits or symbols(s)" output from the encoder 62 in McCallister's FIG. 3) (i.e., McCallister's puncturing is then performed after the Examiner-characterized rearranging).

In contradistinction, the Applicant claims subject matter including, among other subject matter limitations, encoding a plurality of information bits, thereby generating a plurality of encoded bits; puncturing at least one of the plurality of encoded bits thereby generating a non-punctured plurality of bits; rearranging an order of the non-punctured plurality of bits, thereby generating a sequence of discrete-valued modulation symbols.

In addition, on page 17-18 of the office action, the Examiner states:

"Although, McCallister et al. does not specifically teaches that puncturing at least one of the plurality of encoded bits before rearranging the order of the plurality of encoded bits; however it would have been obvious to one of ordinary skilled in the art at the time that invention was made to perform puncturing at least one of the plurality of encoded bits before rearranging the order of the plurality of encoded bits. Moreover, in the arguments filed on 10/06/2008, on page 12 and 13 the applicant clearly states that "Moreover, the Applicant respectfully asserts that one having skill in the art to which the invention pertains, **if provided the Applicant's originally filed specification (including figures and written description)**, would properly understand that (1) rearranging of encoded bit could be effectuated before the puncturing of the rearranged encoded bits or (2) puncturing of the encoded bits could be performed before rearranging an order of the non-punctured (i.e. remaining) encoded bits as well. This may be clearly understood in dependent claims 25-28". Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to perform puncturing at least one of the plurality of encoded bits before rearranging the order of the plurality of encoded bits as taught by McCallister et al. in the Cherubini et al. system and method in order to removes predetermined bits from the encoded bit stream and appropriately restructures the encoded bit stream by delaying certain encoded bits as necessary." (**emphasis added**)

It appears that the Examiner has made a gross mischaracterization of the Applicant's comments in the previous filing.

The Applicant stated that, "if provided the Applicant's originally filed specification (including figures and written description)", then "one having skill in the art to which the invention pertains" "would properly understand" the Applicant's claimed subject matter.

In other words, "one having skill in the art to which the invention pertains" "would properly understand that (1) rearranging of encoded bit could be effectuated before the puncturing of the rearranged encoded bits or (2) puncturing of the encoded bits could be performed before rearranging an order of the non-punctured (i.e. remaining) encoded bits as well" "if provided the Applicant's originally filed specification (including figures and written description)".

It appears that the Examiner fails to consider the qualification of "if provided the Applicant's originally filed specification (including figures and written description)" when considering the Applicant's comments filed on 10/06/2008.

It is clear in the Applicant's comments, as qualified by "if provided the Applicant's originally filed specification (including figures and written description)", that such teaching and disclosure as identified by the Applicant is in fact included within "the Applicant's originally filed specification (including figures and written description)"; this is in no way any statement that such subject matter included within Applicant's originally filed specification (including figures) is obvious.

These comments provided by the Applicant in the previous filing merely show that the Applicant did in fact disclose this claimed subject matter and that it is supported in the "DETAILED DESCRIPTION OF THE INVENTION", which is clearly not a prior art section.

Again, the Examiner apparently failed to consider the qualification of "if provided the Applicant's originally filed specification (including figures and written description)" in the Applicant's comments.

The Applicant's originally filed specification (including figures) teaches and discloses the described subject matter. The Applicant did not comment in any way that such subject matter is obvious to one having skill in the art to which to which the

invention pertains, but rather that it is enabled and described therein so that "one having skill in the art to which to which the invention pertains, if provided the Applicant's originally filed specification (including figures and written description), would properly" understand the subject matter.

The Applicant stated that the Applicant's originally filed specification (including figures) teaches and discloses this subject matter, and the Applicant most certainly did not state that such subject matter was in any way obvious.

The Applicant also respectfully asserts that the inclusion of Cherubini does not overcome the deficiencies of McCallister.

In view of at least these comments made above, the Applicant respectfully believes that these independent claims rejected above are patentable over these cited references.

The Applicant respectfully believes that these dependent claims rejected above, being further limitations of the subject matter as claimed in allowable independent claims, respectively, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejections of these claims.

The Applicant respectfully believes that the pending claims are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present U.S. utility patent application.

RESPECTFULLY SUBMITTED,

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